**Dr. M C Bhuvaneswari**
**Associate Professor**
**Department of Electrical & Electronics Engineering**
**PSG College of Technology, Coimbatore – 641 004**
***e-mail:***

## EDUCATION

**DOCTORATE**

(Month/Year) VLSI Design and Testing
Bharathiar University

**POSTGRADUATE**

(Month/Year) Applied Electronics
Bharathiar University

**UNDERGRADUATE**

(Month/Year) Electronics and Communication Engg.
Madras University

## EXPERIENCE

Teaching: 27 Years
Research: 20 Years

## COURSES HANDLED

**UNDERGRADUATE**

- Digital System Design
- VLSI Design
- Digital Signal Processing
- Microprocessor based System Design
- Electric Circuits
- Electronic Devices
- Network Theory
- Digital Electronics
- Electronic Circuits
- Personal Computer Systems

- Microprocessor Technology
- C Programming
- Data Processing

**POSTGRADUATE**

- Algorithms for VLSI Design Automation
- VLSI Testing and Testability
- Digital System Design and Testing
- ASIC Design

## RESEARCH AREAS

- Applied Electronics
- VLSI Design and Testing
- Genetic Algorithms
- Digital System Design
- Microprocessors
- Multi-objective optimization.

## PUBLICATIONS

### i) Book Chapter:

"Simulation Based ATPG for Crosstalk Delay Faults in VLSI Circuits using Genetic Algorithm" is a book Chapter in the book titled "Genetic Algorithms Theories and Applications",
**Paperback:** 352 pages,
**Publisher:** LAP LAMBERT Academic Publishing (March 22, 2012),
**Language:** English,
**ISBN**-10: 3848447088,
**ISBN**-13: 978-3848447084,

**ii) Book titled** "Application of Evolutionary Algorithms for Multi-Objective Optimization
in VLSI and Embedded systems" ,2015.

A. National / International Conferences : 40

B. National / International Journals : 34

**International Journal**


[01] M C Bhuvaneswari and S N Sivanandam, " Simulation of Asynchronous Sequential Circuits using Fuzzy Delay Model", AMSE Journal: General Physics and Electrical Applications, Vol. 76, No.8, Dec. 2003, pp. 55 - 69.

[02] M C Bhuvaneswari and S N Sivanandam, "Testing Asynchronous circuit using Synchronous Test Model", AMSE Journal: General Physics and Electrical Applications,Vol. 78,No.2,2005,Pg.57-67.

[03] M.Jagadeeswari and M.C.Bhuvaneswari, "A Multi-Objective Genetic Algorithm for Hardware-Software Partitioning in Embedded Systems: A Weighted-Sum Approach", International Journal of Advances in Computer Science and Engineering, vol.1, No. 3, Nov.2007, pp. 249-261.

[04] M.C.Bhuvaneswari, M Jagadeeshwari, " A Fast Multi-Objective Genetic Algorithm for Hardware-Software Partitioning in Embedded System Design", ICGST International Journal on Artificial Intelligence and Machine Learning",Vol.8,Issue.II,Dec.2008, pp17-23

[05] M Shanthi and M.C. Bhuvaneswari, " Design of CMOS Operational Amplifier using Multiobjective Genetic Algorithms", International Engineering and Technology Journal of Advanced Computing,Vol.3, No. 1, 2009, pp 8-11.

[06] M.Jagadeeswari and M.C.Bhuvaneswari, "Efficient multi-objective genetic algorithm for hardware-software partitioning in embedded system design: ENGA", International Journal of Computer Applications in Technology, Vol. 36, No.3/4 ,2009 pp. 181 – 190.

[07] M.Jagadeeswari and M.C.Bhuvaneswari, "Binary Particle Swarm Optimization Algorithm for Functional Partitioning of Embedded Systems". CIIT International Journal of Programmable Deice, Circuits and Systems, Vol.1, No.1, April 2009, pp.1-6.

[08] M Shanthi and M.C. Bhuvaneswari, "Design Optimization Methodology for CMOS Operational Amplifier using NSGA-II", CIIT International Journal of Programmable Deice, Circuits and Systems, Vol.1, No.1, April 2009, pp.7-12.

[09] R Indumathy and M C Bhuvaneswari," Non-Dominated Sorting Genetic Algorithm-II based Timetabling Algorithm", International Engineering and Technology, Journal of Information Systems", Vol.3, No.1, 2009, pp.18-23.

[10] S.Jayanthy, M.C.Bhuvaneswari, " Simulation Based ATPG for Crosstalk Delay Faults in VLSI Circuits Using Genetic Algorithm" ,ICGST –AIML Journal,ISSN:1687-846,Vol.9,Issue2,Dec. 2009, pp11-17.

[11] G Subashini and M C Bhuvaneswari, " A Fast and Elitist Bi-objective Evolutionary Algorithm for Scheduling Independent Tasks on Heterogeneous Systems", ICTACT Journal on soft computing, July 2010,Issue 01,pp 9-17.

[12] G.Subashini, PU.Nivetha, M.C.Bhuvaneswari, "A Bi-Objective Evolutionary Algorithm for Fault Tolerant Scheduling in Heterogeneous Systems", *International Journal of Computational Intelligence Research*, Vol 6-4, Dec 2010, pp 939-945.

[13] G. Subashini , M.C. Bhuvaneswari, "NSGA - II with Controlled Elitism for Scheduling Tasks in Heterogeneous Computing Systems", *International Journal of Open Problems in Computer Science and Mathematics.,* Vol. 4, No. 1, March 2011, pp 214-227.

[14] G. Subashini , M.C. Bhuvaneswari, "Non Dominated Particle Swarm Optimization For Scheduling Independent Tasks On Heterogeneous Distributed Environments" , *International Journal of Advances in Soft Computing and Its Applications,* Vol. 3, No. 1, March 2011, pp 1-17.

[15] G. Subashini , M.C. Bhuvaneswari, "Dynamic NSPSO For Task Scheduling On Heterogeneous Systems", *International Journal On Computer Engineering And Information Technology,* Vol. 24, No. 1, June –August 2011, pp 22-30.

[16] S.Jayanthy, M.C.Bhuvaneswari, "Simulation based Low power Test Generation for Crosstalk delay Faults" *International Journal of Modelling &Simulation*, *ISSN: 0288-6203*, Volume 31, No. 3, 2011

[17] S.Jayanthy, M.C.Bhuvaneswari, "An efficient multi-objective genetic algorithm for low power testing of crosstalk delay faults in VLSI circuits", Advances in Modeling and Simulation Techniques in Enterprises [AMSE], Vol. 54 ,Issue2 , 2011,pp 28-48.

[18] Jayanthy, S., Bhuvaneswari, M.C. and Sujitha, Keesarapalli. "Test Generation for Crosstalk-Induced Delay Faults in VLSI Circuits using Modified FAN algorithm", VLSI Design, Vol. 2012, Article ID 745861, 10 pages, 2012, doi:10.1155/2012/745861

[19] S. M. Logesh, D. S. Harish Ram and M. C. Bhuvaneswari, "A Survey of High-Level Synthesis Techniques for Area, Delay and Power Optimization", International Journal of Computer Applications, Vol 23, No.10, 2011

[20] M.Jagadeeswari and M.C.Bhuvaneswari, "Estimation of HW/SW Cost Parameters in Altera FPGA Design Environment", WSEAS Transactions on Information Science and Applications,Issue 11, Vol.8, Nov.2011.

[21] G. Subashini , M.C. Bhuvaneswari," Task Allocation in Distributed Computing Systems using Adaptive Particle Swarm Optimization", International Journal of Computer Applications and Technology, Vol.44,No.4 pp293-302,2012.

[22] G. Subashini , M.C. Bhuvaneswari," Comparison of Multi-objective Evolutionary Approaches for Task Scheduling in Distributed Computing Systems," Sadhana, Vol.37,No.6, pp 675-694,2012.

[23] D. S. Harish Ram, M. C. Bhuvaneswari, and Shanthi S. Prabhu, "A Novel Framework for Applying Multiobjective GA and PSO Based Approaches for Simultaneous Area, Delay, and Power Optimization in High Level Synthesis of Datapaths," VLSI Design, vol. 2012, Article ID 273276, 12 pages, 2012. doi:10.1155/2012/273276,Jan.1012.

[24] Rajkumar, P., Bhuvaneswari, M.C."Investigation of Segmentation Techniques in Microarray Data Analysis", European Journal of Scientific Research (EJSR). Vol. 96,
No. 2, pp. 274 - 284, February 2013.

[25] Jayanthy, S., Bhuvaneswari, M.C. and Prabhu.M "Simulation based ATPG for low power testing of crosstalk delay faults in Asynchronous Circuits". International Journal. Computer Applications in Technology, Vol. 48, No. 3, 2013, pp 241-252.[Inderscience Publishers 09528091]

[26] RAM, D. S. H., BHUVANESWARI, M. C., UMADEVI, S. "Improved Low Power FPGA Binding of Datapaths from Data Flow Graphs with NSGA II -based Schedule Selection" International Journal of Advances in Electrical and Computer Engineering,Vol.13,issue4,2013, pp. 85-92.

[27] A Nandhini, M Shanthi and M C Bhuvaneswari. Article: Performance Analysis of 4-bit Flash ADC with Different Comparators Designed in 0.18um Technology. International Journal of Computer Applications (IJCA) Proceedings on International Conference on Innovations In Intelligent Instrumentation, Optimization and Electrical Sciences ICIIIOES(5):, December 2013,pg.1-5

[28] S Jayanthy, and M C Bhuvaneswari "Fuzzy delay model based fault simulator for crosstalk delay fault test generation in asynchronous sequential circuits" *Sadhana* Vol. 40, Part 1, February 2015, pp. 107–119.

[29] A.Gunasundari, M.C. Bhuvaneswari and K.R. Sri Sountharya," Mixed Signal Integrated Circuits Testing Using Wavelets And Neural Networks" Australian Journal of Basic and Applied Sciences, 9(16) Special 2015, pp. 301-305.

[30] Angappan Natarajan and M.C.Bhuvaneswari, "System-on Chip Test Scheduling using Multi-Objective Particle Swarm Optimisation Algorithm" International Journal of Applied Engineering Research, ISSN 0973-4562, Volume 10, Number 3 (2015) pp. 7469-7484.

**National Journal**

[01] M C Bhuvaneswari and S N Sivanandam, "Genetic Algorithm based Test Generation: An Analysis of Crossover Operators", Journal of the Computer Society of India, Vol32. March 2002,pp. 10-17.

[02] M C Bhuvaneswari, S N Sivanandam , "Automatic Test Pattern Generation for Synchronous Sequential Circuits using Guided Genetic Algorithm", Technology Journal, Dec 2003, pp. 65-68.

[03] M C Bhuvaneswari and S N Sivanandam, " New Crossover operator for GA based Synchronous Sequential Circuit Testing", Indian Journal of Engineering and Material Sciences, Vol. 10, Feb. 2003, pp. 21-26.

[04] M.Jagadeeswari and M.C.Bhuvaneswari., "Hardware-Software Functional Partitioning of Embedded Systems Using Genetic Algorithms", Journal of Computer Science, Volume 03, issue 04, May-June 2009, ISSN 0973-2926.

**International Conference / Workshop**

[01] M C Bhuvaneswari, N. Gokul and S N Sivanandam, " Application of Differential Evolution Algorithm to VLSI Sequential Circuit Test Pattern Generation," International Conference On Robotics vision and Parallel Processing for Automation, June 1999, Malaysia.

[02] M C Bhuvaneswari and S N Sivanandam, "Testing of Asynchronous Circuits – A Survey," International Workshop on VLSI Design and Test, August 1999, New Delhi.

[03] M C Bhuvaneswari , S N Sivanandam and S P SreeVidya, " Automatic Test pattern generation for Asynchronous Sequential Circuit using Adaptive genetic Algorithms ," International Conference MENDEL 2000, Brno

[04] M C Bhuvaneswari , S N Sivanandam and S P SreeVidya, " Simulation of Asynchronous Sequential Circuits using Novel Fuzzy Delay Model ," International Conference on Modeling and Simulation, September 2000, Spain.

[05] M C Bhuvaneswari and S N Sivanandam, " Testing Asynchronous Sequential Circuits Using Synchronous Model", VLSI Design and Test Workshops, August 2000, New Delhi, pp.82-83.

[06] M C Bhuvaneswari, S N Sivanandam and S P Selvaraj , " Testing Asynchronous Sequential Circuit using Guided Genetic Algorithm", International conference: Asia- Pacific Telecom, Advances in telecommunication and Information technology, December 2000, Vellore, pp. 323-329.

[07] M.Jagadeeswari and M.C.Bhuvaneswari, "Hardware/Software Functional Partitioning of Embedded Systems using Genetic Algorithms", Proceedings of International Conference on Advanced Communication Systems, Jan 10-12, 2007, pp. 65-70.

[08] M.C.Bhuvaneswari and M Shanthi, "Design Of Analog CMOS Operational Amplifiers using Multiobjective Genetic Algorithms", Proceedings of International Conference on Modelling and Simulation, Aug. 2007, Volume 3,pp. 54

[09] M.Jagadeeswari and M.C.Bhuvaneswari, "Fast Elitist Non-Dominated Sorting Genetic Algorithm for Hardware-Software Partitioning", Proceedings of 2nd International Conference on Intelligent Systems and Control, Feb 1-2, 2008, pp103

[10] M.C.Bhuvaneswari and M Shanthi, "Particle Swarm Optimizer for CMOS operational amplifier synthesis" Proceedings of the International Conference in Advanced Computing and Communication Techniques for High Performance Applications, Vol.2,2008,pp.710-714.

[11] S.Jayanthy, M.C.Bhuvaneswari, J.Sathish Kumar, "Test Generation in VLSI Circuits for Crosstalk Delay Faults using Genetic Algorithm", Proceedings of the International conference on Communication Technologies and VLSI Design(Commv 09),Oct2009, pp 253-256.

[12] Rajkumar, P.,Bhuvaneswari, M.C. and Nirmalakumar, K. "A Novel Method for Cancer Level Identification using Microarray Data", Fourth National Conference on Signals, Systems and Security (NCSSS-2010), Bannari Amman Institute of Technology, February 26-27,2010.

[13] S.Jayanthy, M.C.Bhuvaneswari, G.Harihara Sudan, "Test Pattern Generation for Crosstalk Delay Faults in VLSI Circuits" Proceedings of the International Conference on Intelligent Design and Analysis of Engineering Products, Systems and Computation, July 9-10,2010

[14] S.Jayanthy, M.C.Bhuvaneswari, G.Renisha, "Multiobjective Genetic Algorithm for Testing of crosstalk delay faults in VLSI Circuits" Proceedings of the International conference on Embedded systems, July 14-16, 2010

[15] S.Jayanthy, M.C.Bhuvaneswari, M.Prabhu, "Multiobjective Genetic Algorithm for Testing of crosstalk delay faults in VLSI Circuits: Weighted sum approach" Proceedings of the International Conference on Innovative Research in Engineering and Technology, August 12-14, 2010.

[16] G. Subashini , M.C. Bhuvaneswari, "A Fast and Elitist Multi-objective Genetic Algorithm for Scheduling Independent Tasks on Distributed Heterogeneous Systems", In Proceedings of the International Conference on Embedded Systems, ICES,2010, CIT, Coimbatore.

[17] D. S. Harish Ram, M. C. Bhuvaneswari,, Malarvizhi. K, "A Genetic Algorithm Approach for Multi-objective Power, Area and Delay Optimization For Behavioral Synthesis of Data Flow Graphs, International Conference on Embedded Systems, ICES 2010, CIT, Coimbatore, July 14-16, 2010.

[18] S.M. Logesh, D.S. Harish Ram, M.C. Bhuvaneswari, *Multi-objective Optimization of Power, Area and Delay during High-Level Synthesis of DFG's - A Genetic Algorithm Approach*, International Conference on Electronic Computer Technology, ICECT 2011, Kanyakumari, April 8-10, 2011, Vol 1, pp 108-112

[19] G. Subashini , M.C. Bhuvaneswari, "Multi-objective Task Scheduling in Distributed Heterogeneous Computing Systems by Non-dominated Sorting Particle Swarm Optimization", In Proceedings of the International Conference on Innovative Research in Engineering and Technology, iCIRET 2010,Park College of Engineering and Technology, TamilNadu, India.

[20] Subashini G, Nivetha Pu, Bhuvaneswari MC, " A Bi-Objective Evolutionary Algorithm for Fault Tolerant Scheduling in Heterogeneous Systems" , In Proceedings of the International Conference on Computational Intelligence ICCI 2010, G R Govindarajulu School of Applied Computer Technology, TamilNadu, India.

[21] S.Jayanthy, M.C.Bhuvaneswari, M.Prabhu," Multiobjective Genetic Algorithm for low power testing of Crosstalk delay faults in Asynchronous circuits", Proceedings of the International Conference on Emerging Trends in Computing March 17-18,2011

[22] D. S. Harish Ram, M. C. Bhuvaneswari, S. M. Logesh, A Novel Evolutionary Technique for Multi-Objective Power, Area and Delay Optimization in High Level Synthesis of Datapaths, 2011 IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2011, Chennai, July 4-6, 2011, pp 290-295.

[23] Karthi, S.P., Shanthi, M., Bhuvaneswari, M.C. "Parametric Fault diagnosis in analog circuit using Genetic Algorithm" In Proceedings of the International Conference on Green Computing, Communication and Electrical Engineering (ICGCEE-2014) , on 6th -8th March ,2014 .

[24] D.Priya., Shanthi, M., Bhuvaneswari, M.C."Polynomial coefficients Based Parametric Fault diagnosis for analog Circuits" In abstract proceedings Of the International Conference on Electrical, Instrumentation and Communication Engineering Recent Trends and Research Issues( ICE2- RTRI 2015) on 2nd & 3rd January 2015

**National Conference / Workshop**

[01] M C Bhuvaneswari, N Srimannarayanan and S N Sivanandam," A Rule-based Approach for Reducing Single Output Boolean Function using Reduction Operator", National Seminar on Knowledge based system, Saradar Patel University, Gujarat, during 3-4 June 1998.

[02] M C Bhuvaneswari and S N Sivanandam, " Event-Driven Simulation of Asynchronous Sequential Circuits using Novel Fuzzy Delay Model", Proceedings of the National Conference on Recent Trends in Advanced Computing, February 2000, Thirunelveli, pp. 125-129.

[03] M C Bhuvaneswari , S N Sivanandam and S P SreeVidya, " Testing of VLSI Asynchronous Sequential Circuits using Genetic Algorithms," National Symposium on Intelligent measurement and control (NSIMC -2000), February 2000,Chennai, pp. 110-117.

[04] M C Bhuvaneswari and S N Sivanandam, "Simulation Based Technique for Testing Asynchronous Sequential Circuits," 24th National Systems Conference, December 2000, Bangalore, pp. 434-440.

[05] M C Bhuvaneswari, S N Sivanandam and S P Selvaraj , "A New Crossover Operator for GA Based Test Pattern Generator for Synchronous Sequential Circuits," National Conference on Technology Convergence for Information Communication and Entertainment - NICE 2000, February 2001, Cochin, pp. 152-155.

[06] M C Bhuvaneswari and S N Sivanandam, "Parallel Guided Genetic Algorithm based Test pattern Generator using Message Passing Interface," VLSI Design and Test Workshops, August 2001,Bangalore, pp.341-342.

[07] M C Bhuvaneswari , "Design, Simulation and Synthesis of a Fuzzy Controller using VHDL", VLSI Design and Test Workshops, August 2002,Bangalore, pp.104-108.

[08] M Jagadeeswari and M C Bhuvaneswari, "Hardware-Software Partitioning for Embedded System Design", National Conference on Emerging Trends in Instrumentation Systems, Jan 2006, pp. 164 – 170.

[09] M.C.Bhuvaneswari and G Madhavi, " Low power Test Pattern Generation for Sequential Circuits using Non-dominated sorting GA", Proceedings of the third National Conference on Optimization Techniques in Engineering Sciences and Technologies, March 27-28,2008, ppE1-5.

[10] M.C.Bhuvaneswari, M Jagadeeshwari and P Rajasekar, "Low power Hardware-Software Partitioning for Embedded System using GA", Proceedings of the third National Conference on Optimization Techniques in Engineering Sciences and Technologies, March 27-28, 2008, ppE6-10.

[11] M.C.Bhuvaneswari and M Shanthi, "Elitist Non-Dominated Sorting Genetic Algorithm for CMOS OP-AMOP Synthesis" Proceedings of the National Conference Advances in Communication and Computing, April 2008.

[12] M.Jagadeeswari and M.C.Bhuvaneswari, "Multi-Objective Particle Swarm Optimization for Hardware-Software Partitioning", Proceedings of the National Conference on Adaptive Sensors & Intelligent Systems NCASIS'08, Nov 21-22, 2008, pp 186-191.

[13] S.Jayanthy, .M.C.Bhuvaneswari, T.kavitha "Simulation Based ATPG For Path Delay Faults In Digital Circuits Using Genetic Algorithms", Proceedings of the National Conference on Adaptive Sensors & Intelligent Systems NCASIS'08, Nov.21-22, 2008, pp 80-84.

[14] G. Subashini and M.C. Bhuvaneswari "A multiobjective evolutionary algorithm for scheduling independent tasks in a multiprocessor system" , Proceedings of the Fourth National Conference on Innovations in Information and Communication Technology, 2008,pp.122-127.

[15] G. Subashini , M.C. Bhuvaneswari, "Multiobjective Particle Swarm Optimization For Load Balancing In Distributed Computing Systems", In Proceedings of the

National Conference on Intelligent Information Retrieval , 2010, PSG College of Technology, Coimbatore.

[16] Karthi, S.P., Shanthi, M., Bhuvaneswari, M.C. "Evolutionary Technique for fault diagnosis in analog circuits using transfer function." In abstract proceeding of National Conference on Electronics, Signal processing, communication and Embedded systems (NCESCES'14) on 27-28 Febrauary,2014.

## SEMINARS / CONFERENCES ORGANISED

- Short term course on VLSI Design and VHDL, 19-21, Feb. 2000
- Short term course on VLSI Design and VHDL, 16-17,23-24, Dec.2000
- Workshop on mixed signal VLSI design and test, 2-3, Dec.2005, Sponsored by VLSI society of India.
- Workshop on mixed signal VLSI design and test, 2-3, Apr,2007, Sponsored by VLSI society of India.
- National Symposium for Post- Graduate Students NSPGS 2010
- National Conference on Recent Trends in Electrical and Electronics Engg.,( for PG Students), Apr. 2011
- One Credit Course on Digital Design with Verilog HDL, Feb 2011
- One Credit Course on CAD Tools for VLSI Design Automation, Sept. 2011
- National Conference on Recent Trends in Electrical and Electronics Engg.,( for PG Students), Apr. 2012
- One credit course on 'digital system design using verilog HDL' in Collaboration with Analog Devices, Bangalore, Feb. 2014
- Training Programme on MicroWind : A VLSI layout and Simulation Tool.Feb. 2014.
- National Workshop on ' VLSI LAYOUT DESIGN' in Association with ni logic, Pune, Mar. 2014.
- One credit course on 'digital system design using verilog HDL' in Collaboration with Analog Devices, Bangalore, Aug. 2015.

## SEMINARS / CONFERENCES ATTENDED

| S. No. | Particulars | Course Title | Duration | No. of Days | Venue |
|---|---|---|---|---|---|
| 1. | ISTE sponsored Summer School | Computer Integrated manufacturing | 7-06-1992 to 20-06-1992 | 14 | PSG College of Technology |
| 2. | Project IMPACT- | Digital Systems | 02-11-1992 | 52 | IISc,Bangalor |

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|---|---|---|---|---|---|
| | Instruction Enhancement Programme | | to 23-12-1992 | | e |
| 3. | ISTE Winter School | Wind and Solar Electric Power Generation and Conversion | 14-11-1994 to 26-11-1994 | 13 | PSG College of Technology |
| 4. | ISTE Short term Course | Digital ASIC Design | 28-11-1994 to 09-12-1994 | 12 | IIT, Madras |
| 5. | ISTE Winter School | Relational Database management System | 17-02-1997 to 14-03-1997 | 28 | PSG College of Technology |
| 6. | Sponsored by VLSI Society of India | VLSI Design and Test Workshops | 6-08-98 to 7-08-98 | 2 | New Delhi. |
| 7. | Sponsored by IMPACT , DOE, India | VLSI Design and VHDL | 07-12-98 to 25-12-98 | 19 | IIT ,New Delhi. |
| 8. | National Conference organized by Manonmaniam Sundranar University | Recent trends in Advanced Computing | 11-2-2000 to 12-2-2000 | 2 | Thirunelveli |
| 9. | Sponsored by VLSI Society of India | VLSI Design and Test Workshops | 25-8-2000 to 27-8-2000 | 3 | New Delhi. |
| 10. | National Conference Sponsored by System Society of India | 24th National System Conference | 7-9-2000 to 9-9-2000 | 3 | ISRO, Bangalore |
| 11. | Short term Course | VLSI Design and VHDL | 16-17 and 23-24, Dec 2000 | 4 | PSG College of Technology, Coimbatore |

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|---|---|---|---|---|---|
| 12. | Sponsored by VLSI Society of India | VLSI Design and Test Workshops | 16-8-2001 to 18-8-2001 | 3 | IISC, Bangalore |
| 13. | Workshop Conducted by ECIL | VLSI Design and Verilog HDL | 20-9-2001 to 22-9-2001 | 4 | ECIT, Coimbatore |
| 14. | AICTE / ISTE Short term course | Wired and wireless Computer Communication | 10-11-02 to 23-11-02 | 14 | PSG College of Technology, Coimbatore. |
| 15. | FDP Sponsored by AICTE | Introduction and applications of neuro Fuzzy Genetic Systems | 17.12.2006 to 30.12.2006 | 14 | PSG College of Technology. |
| 16. | FDP Sponsored by TEQIP II | Non Traditional Optimization Techniques for research and Industrial needs | 09.10.2012 to 15.10.2012 | 7 | Government College of Technology, Coimbatore |
| 17. | FDP Sponsored by AICTE | Verification and Testing of VLSI Circuits | 06.11.2013 to 19.11.2013 | 14 | PSG College of Technology. |
| 18. | FDP Sponsored by TEQIP II | Digital and Analog VLSI Design | 20.11.2013 to 26.11.2013 | 7 | Coimbatore Institute of Technology. |
| 19. | FDP Sponsored by TEQIP II | Real-Time Embedded Systems and Internet of Things(IoT) | 22.06.2016 To 28.06.2016 | 7 | PSG College of Technology |
| 20. | Two day workshop | Question paper setting | 07.01.2011 o 08.01.201 | 2 | PSG College of Technology |

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| 21. | Three day staff development programme | Staff Development Programme | 28.01.2012 &16.03.2012 &17.03.2012 | 3 | PSG College of Technology |
| 22. | Workshop Sponsored by TEQIP II | Preparation of Technical Reports for PG laboratories | 08.10.2013 | 1 | PSG College of Technology |
| 23. | MCEP Sponsored by TEQIP II | Academic Leadership and Excellence | 24.10.2013 | 1 | PSG College of Technology |
| 24. | International Conference sponsored by VLSI society of India, IEEE | VLSI design and embedded systems, Bangalore | 8-01-2007 to 10-01-2007 | 3 | Bangalore |

## SPECIAL LECTURES DELIVERED

| PROGRAMME | DURATION | PERIOD | NATURE OF INVOLVEMENT |
|---|---|---|---|
| VLSI Awareness Workshop, VLB College of Engineering and Technology | 1 ½ days | 23 - 02- 2007 | Introduction to VLSI Testing |
| Workshop on Mixed Signal VLSI Design and Test, PSG College of Technology | 1 days | 02-12-05 | VLSI Testing using GA |
| 2nd Workshop on Mixed signal VLSI design and test, PSG College of Technology | 1 ½ days | 25-04-2007 | VLSI Testing using Evolutionary algorithms |
| Workshop on Computational Optimization and Modeling | 2 days | 21.01.2011 to 22.01.2011 | Delivered Lecture on Multi Objective Evolutionary Techniques |
| TEQIP sponsored one week faculty development programme on embedded and real | 7 days | 12.10.2014 to 18.10.2014 | Delivered Lecture on Hardware/ Software Partitioning (17.10.2014) |

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| time software and systems, PSG Tech. | | | |
| AICTE _ QIP sponsored one week short term course on research challenges in vlsi design and testing, CIT, Coimbatore | 7 days | 08.12.2014 to 14.12.2014 | Delivered Lecture on VLSI testing (12.12.2014) |
| AICTE sponsored Summer School on Recent Trends in Embedded Computing System Design, SREC, Coimbatore | 2 Weeks | 11.05.2015 To 24.05.2015 | Delivered Lecture on Hardware/ Software Co-design (19.05.2014) |

## AWARDS

- Dakshinamoorthy Award for Teaching Excellence – 2010

## MEMBERSHIP OF PROFESSIONAL BODIES

- Life Member of Indian Society for Technical Education
- Life Member of Institution of Engineers (India)
- Life Member of Computer Society of India
- Life Member of System Society of India

## DOCTORAL GUIDANCE / SUPERVISION

No. PhD Guided : completed - 3 ; on going - 3

No. MS ( By Research) : completed - 1

No. of PG projects Guided : 52